AMENDMENT TO THE SPECIFICATION

Please add the following new paragraph at page 18, line 20, after the paragraph that ends "...about 310 °C for a few minutes" and before the paragraph that begins "The present invention..." Support for this new paragraph is found throughout the Specification and, in particular, at page18, lines 14-15, and in Claim 2. *See* MPEP 608.01(l).

In FIG. 7 is shown an additional stacked layer on the thin chip **240**, the additional stacked layer comprising a stacked interconnect layer **230'** on the top surface of the thin upper chip **240**, the stacked interconnect layer **230'** comprising a compliant dielectric material **231'** and an interconnect structure embedded in the compliant dielectric material **231'**, the interconnect structure comprising one or more via capture pads **232'** connected to the associated input/output pads **243** on the top surface of the thin upper chip **240**; and a stacked thin chip **240'** on the stacked interconnect layer **230'**, the stacked thin chip **240'** comprising one or more microsystem devices **242'** with associated input/output pads **243'** on the top surface of the stacked thin chip **240'** that are connected to the one or more via capture pads **232'** in the stacked interconnect layer **230'** by conductive vias **244'** through the stacked thin chip **240'**. Additional thin chip and interconnect layers can be stacked on the stacked thin chip **240'** using the wafer-stacking method.

Please add the following new paragraph at page 8, line 23, after the paragraph that ends "...formed after the two wafers are bonded together" and before the section that begins "DETAILED DESCRIPTION OF THE INVENTION".

FIG. 7 shows a cross-sectional side view of a singulated stacked chip comprising a thick bottom wafer, a thin upper chip, and a stacked thin chip.